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An Original Hybrid Multilevel DC-AC Converter Using Single-Double Source Unit for Medium Voltage Applications: Hardware Implementation and Investigation

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ABSTRACT In this article, an original hybrid multilevel DC-AC converter configurations are proposed by using single-double source unit for medium voltage applications. The proposed topologies are derived by hybridization of single and double source units with polarity changer and cascaded with full-bridge converter for medium and high voltage applications. Two different hybrid topologies presented and each topology configured for both symmetric and asymmetric method. The proposed hybrid topologies compared with the conventional cascaded H-bridge converter (CHB), and the best topologies recommended for medium voltage applications. The comparison in terms of the number of switches, gate driver circuits, maximum blocking voltage by switches and total peak inverse voltages of switches presented. The proposed topologies require a small installation area and low cost. The validity of the proposed hybrid converter structures is verified by simulation using MATLAB/Simulink and hardware results. The simulation and hardware results show a good agreement with the theoretical approach.

INDEX TERMS Harmonics distortion, multilevel converters, hybrid converter topology, power switches, symmetric and asymmetric inverter.

I. INTRODUCTION

Multilevel DC-AC converters are the preferred choice of a power converter in medium voltage and high power applications. Generally, the multilevel converters generated staircase output voltage with several D.C. source as input [1]–[3]. The multilevel converter has numerous advantages over two-level inverter like low output voltage total harmonic distortion (THD), low Electromagnetic Interference (EMI), reduced the size of L.C. filter, low *dv/dt* stress and overall higher efficiency [4]–[8]. The three primary conventional multilevel converters are Neutral Point Clamped (NPC), Flying Capacitor (F.C.) and Cascaded H-bridge (CHB) multilevel inverter. The main advantage of Neutral Point Clamped (NPC) topology is that it is more suitable for back to back operation in HVDC applications. However, NPC has some drawbacks including the following: 1) it generates output voltage equals half of the input voltage; it requires additional circuits for voltage balancing of DC-link capacitor, and 3) it uses high number of power diode [9]. Flying capacitor (F.C.) [10] converter topology produces full input voltage at the output, but this topology uses a large number of DC-link capacitor to

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achieve a high number of output voltage levels. Furthermore, the reliability of the converter is reduced due to the large number of capacitors used in this design. Cascaded H-bridge converter (CHB) [11]–[13] topology is attractive due to their modular structure and more redundant state. This topology consists of a series connection full-bridge two-level inverter with isolated D.C. source, and it does not require any additional power electronic components. This topology configured as symmetric and asymmetric methods. In the symmetric configuration, the magnitude of all the dc sources are equal and results in a large number of power electronic switches to obtain the high number of output voltage which is not the case in an asymmetric configuration where the magnitude of D.C. source can determine in geometric progression (binary and trinary method). Therefore, it requires fewer switches to generate a high number of voltage levels. Generally, the conventional multilevel inverter topology always requires the high number of switches to generate a higher number of output voltage levels. As a result, the switching pulse generation is sophisticated, the installation area is large, and the total cost of the converter is high.

New symmetric multilevel converter, non-isolated dc sources with bidirectional switches presented [14]. This converter topology uses various voltage ratings of power switches. It can be extended to n number of sources and required n number of the various voltage rating of switches. A new semi-cascaded inverter is proposed in [15], which configured in both symmetric and asymmetric configuration. However, this topology requires a large number of power switches and its maximum blocking voltage is relatively high. Another non-isolated dc source with bidirectional switches presented in [16]. A large number of switches reduced in this topology, but it requires various voltage rating of power switches which increase the cost of the converter. Besides, it is not a viable solution for high voltage applications due to more voltage stress across the full-bridge switches. For utilize this topology in high voltage applications, the full-bridge converter cascaded with symmetric topology. However, these topologies are not suitable for high voltage applications due to high voltage stress of switches. Motivated by the above discussion, and to increase efficiency and reduce the number of switches and a variety of dc sources for high voltage application, two-hybrid converter topologies presented in this article.

The proposed topology has the following advantages:

- The proposed topology generates a higher number of voltage level with fewer power switches count, which further reduces the number of gate driver circuits, heat sink, size and layout of the circuit.
- The voltage stress on full-bridge switches reduced.
- The proposed hybrid topology I have high modularity.
- In the asymmetric configuration, the number of isolated dc sources reduced.
- The number of ON state switches are less, which leads to a more reduction in power loss.

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

A new multilevel converter with a smaller number of power switches proposed by using single and double source unit. The series/parallel combination of switches connected with single and double source unit. The single source unit consists of one dc source connected with series/parallel combination of power switches, and standing voltage of the switch is V_{dc}. In double source unit, two dc sources connected along with series/parallel switches, but the standing voltage of switches is $2V_{dc}$. The multilevel structure constructed with a combination of both single-double source units (SDS Unit) as shown in Fig. 1, and the 13-level output voltage and current waveforms shown in Fig. 2. The basic unit consists of n number of dc sources, and all these source magnitudes are equal to generate $2n + 1$ level. The full-bridge converter used to produce both positive and negative output voltage, and it withstood for the sum of all the dc source magnitude values. In Table 1, the proposed converter topology is compared with Cascaded H-Bridge (CHB) multilevel inverter. The maximum output voltage $V_{o,max}$ of the proposed topology expressed as,

$$V_{o,max} = \sum_{i=1}^{n} V_i \tag{1}$$

where n denotes the number of isolated dc source presented in the input side. The power loss on a switch is the sum of both

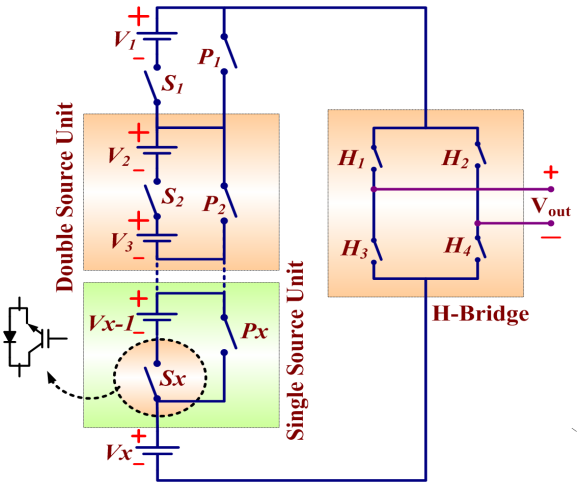


FIGURE 1. Generalized structure of proposed multilevel inverter topology.

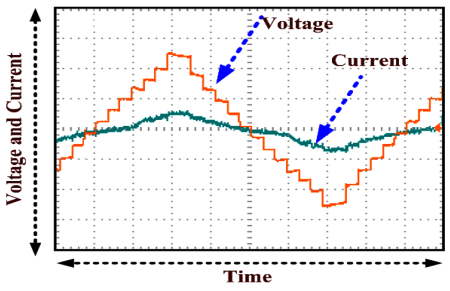


FIGURE 2. 13 level output voltage and current waveform.

switching and conduction losses. The voltage drop across each switch is undesirable. The losses considered while the switch is changed from ON state to OFF state and vice versa. The voltage drops of each switch are assumed to be V_T., the maximum output voltage with power losses calculated as follows,

$$V_{o,max} = \sum_{i=1}^{n} V_i - nV_T \tag{2}$$

III. HYBRID STRUCTURE OF PROPOSED MULTILEVEL CONVERTER

The proposed topology uses a lower number of switches; however, restricted for high voltage applications due to its high voltage stress across the full-bridge converter. For utilizing the proposed topology in high voltage applications, two new hybrid multilevel topologies presented in this section.

A. HYBRID TOPOLOGY I

In hybrid topology, I, the maximum output voltage level is generated with a minimum number of switches. For example, if $n = 4$ considered as the basic unit, then it consists of four dc sources and eight switches with maximum possible of the 9-level output voltage. In this topology, the magnitude of each dc source is equal. This proposed multilevel topology (discussed in section-2) is hybrid with conventional cascaded H-bridge inverter as shown in Fig. 3, in which nU and nL represent the number of dc source presented in the upper leg and lower leg, respectively. The corresponding 27 level output voltage and current waveforms are shown in Fig. 4(a) and Fig. 4(b).

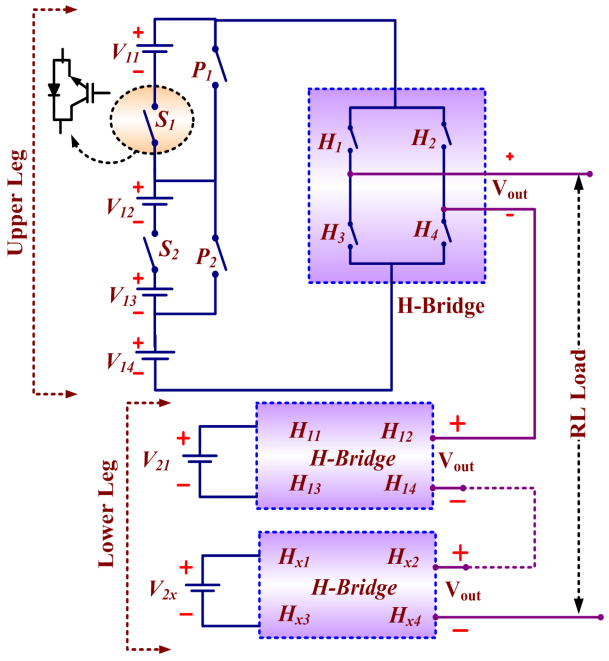


FIGURE 3. Generalized structure of proposed hybrid basic unit with Cascaded H-Bridge (Hybrid Topology I).

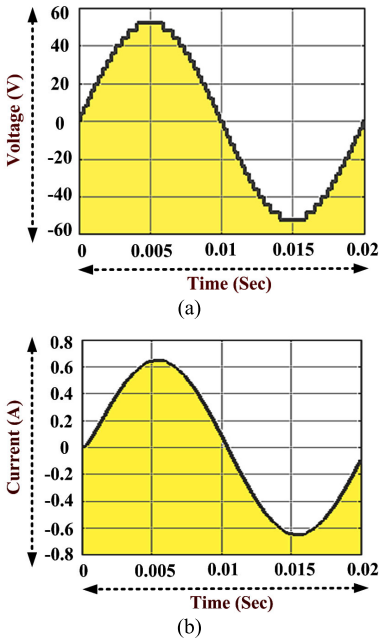


FIGURE 4. Simulation output results of hybrid proposed topology I for 27 Level (a) Voltage waveform (b) Current waveform.

For symmetrical configurations, the magnitude of n number of dc source for both basic unit and CHB is equal, and equations expressed as follows,

$$\begin{pmatrix} V_{11} = V_{12} \\ = V_{13} = V_{14} \end{pmatrix} = V_{dc}; \quad \begin{pmatrix} V_{21} = V_{22} \\ = \ldots\ldots = V_{2n} \end{pmatrix} = V_{dc} \tag{3}$$

For asymmetric configurations, the magnitude of basic unit dc sources is,

$$V_{11} = V_{12} = V_{13} = V_{14} = V_{dc} \tag{4}$$

The magnitude of dc sources for cascaded H-Bridge unit are expressed as follow,

$$\left.\begin{array}{l} 1^{st}\ Unit\ V_{21} = (2nU + 1)^* V_{dc} \\ 2^{nd}\ Unit\ V_{22} = V_{21}{}^*3^* V_{dc} \\ 3^{rd}\ Unit\ V_{23} = V_{22}{}^*3^* V_{dc} \\ k^{th}\ Unit\ V_{2n} = V_{2n-1}{}^*3^* V_{dc} \end{array}\right\} \tag{5}$$

B. HYBRID TOPOLOGY II

The basic unit of the proposed topology is hybrid with the full-bridge converter (Hybrid Topology II) as shown in Fig. 5 and its corresponding simulated 21 level output voltage and current waveforms shown in Fig. 6(a) and Fig. 6(b). For symmetrical configurations, the magnitude of n number of dc source for symmetric topology and the full-bridge unit is equal, and equations expressed as follows,

$$V_1 = V_2 = V_3 = \ldots\ldots V_n = V_{dc}; \quad V_1' = V_{dc} \tag{6}$$

For asymmetric configurations, the magnitude of extended unit dc sources is as,

$$V_1 = V_2 = V_3 = \ldots\ldots . V_n = V_{dc} \tag{7}$$

TABLE 1. Comparison of proposed topology with cascaded multilevel inverter.

Description	Proposed Topology (Fig. 1)	Conventional Cascaded H-Bridge (CHB)
No. of dc source	n	n
No. of switches	$N_{Switch} = \begin{cases} n+5, n = \text{odd} \\ n+4, n = \text{even} \end{cases}$	$4n$
No. of output levels	$2n+1$	$2n+1$
Maximum output voltage	$n*V_{dc}$	$n*V_{dc}$
Maximum blocking Voltage	$n*V_{dc}$	V_{dc}
Total Peak Inverse Voltage	$V_{PIV} = (6n-2)V_{dc}$	$4*n*V_{dc}$

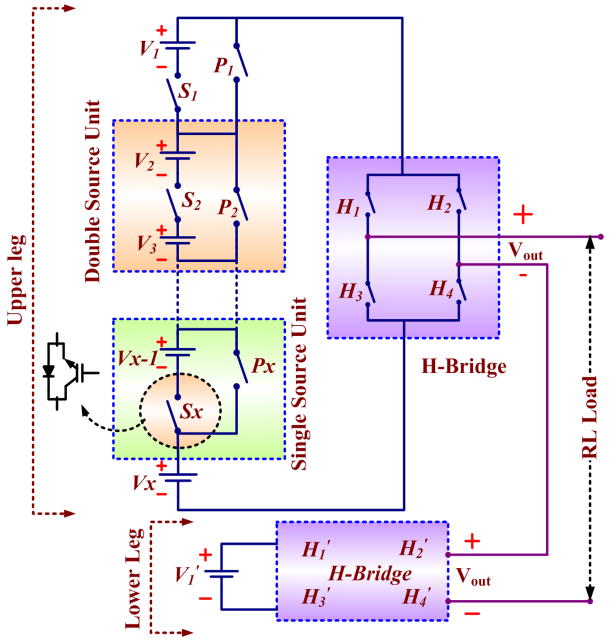


FIGURE 5. Generalized structure of proposed hybrid extended symmetrical topology full bridge (Hybrid Topology II).

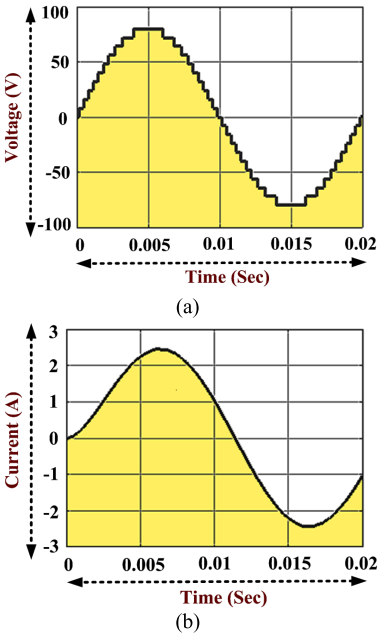


FIGURE 6. Simulation output results of hybrid proposed topology II for 21 level (a) voltage waveform (b) current waveform.

The magnitude of dc sources for full-bridge unit follows,

$$V_1' = 2nU + 1 \tag{8}$$

where nU is the number of dc source in an extended unit of the proposed multilevel inverter. The required number of switches, number of levels, maximum blocking voltage and total standing voltage of switches presented for both symmetric and asymmetric configurations of Hybrid Topology I and II in Table 2 and Table 3, respectively.

IV. COMPARISON OF MULTILEVEL CONVERTERS

The hybrid topology I and conventional CHB multilevel inverter produce very close results in terms of the number of switches and total peak inverse voltage. The number of switches in topology II is lower than the other two topologies, but the total peak inverse voltage is higher in topology II as presented in Fig. 7(a) and Fig. 7(b), respectively. For generate maximum output voltage level with reduced dc source and switches, the asymmetric configurations are preferable, but they require a variety of dc source voltage value and different voltage ratings of switches. Two different methods used to determine the magnitude of dc sources in CHB asymmetric configuration; those are binary (power of 2) and trinary (power of 3) configuration. In this paper, the trinary configuration is considered because it is capable of producing a maximum output voltage level with minimum switches.

For comparisons, the graph of the number of switches (N_{switch}) versus the number of levels (N_{Level}), number of blocks (N_{Blocks}) versus the number of levels (N_{Level}), switch Peak Inverse Voltage (V_{PIV}) versus the number of levels (N_{Level}) and number of switches (N_{switch}) versus switch Peak Inverse Voltage (V_{PIV}) depicted in Fig. 8(a)-8(d), respectively. In Table 4, the symmetric configuration of multilevel inverter compared for maximum output voltage level against equals the power component. In hybrid topology I, maximum blocking voltage of switches is k^{th} cascaded h-bridge unit switches $(2nUL + 1)x(3k-1)V_{dc}$ and basic unit full-bridge converter blocking voltage is $4V_{dc}$. In [17], the auxiliary circuit is hybrid with the full-bridge converter. In this topology, the maximum blocking voltage of switches is higher than the hybrid topology I. The proposed hybrid topology I and CHB Trinary configuration uses the lower number of switches for any given number of voltage levels in comparison with proposed hybrid topology II. The basic unit full-bridge converter has to withstand for a maximum of $4V_{dc}$ whereas in hybrid

TABLE 2. Power component requirements for proposed hybrid topology I.

Description	Topology I (nU=4)	
	Symmetric Configuration	Asymmetric Configuration
Number of Level	$N_{Step} = 2nL + 9$	$N_{Step} = (3^{nL+2})$
Number of Switches	$N_{Switches} = 8 + nL * 4$	$N_{Switches} = 8 + nL * 4$
Number of Gate Driver	$N_{Driver} = 8 + nL * 4$	$N_{Driver} = 8 + nL * 4$
Maximum Blocking Voltage	$V_{Block} = 4 * V_{dc}$	$V_{Block} = \left(\frac{1-3^{nL+2}}{-2}\right) * V_{dc}$
Total Peak Inverse Voltage	$V_{PIV} = (22 + 4nL) * V_{dc}$	$V_{PIV} = \left[4 * \left(\frac{1-3^{nL+2}}{-2}\right) + 6\right] * V_{dc}$

TABLE 3. Power component requirements for proposed hybrid topology II.

Description	Topology II (nL=1)	
	Symmetric Configuration	Asymmetric Configuration
Number of Level	$N_{Step} = 2nU + 3$	$N_{Step} = 3 * (2nU + 1)$
Number of Switches	$N_{Swicth} = \begin{cases} 8, & nU = 1 \\ nU + 9, & nU = \text{Odd}, \quad nU > 1 \\ nU + 8, & nU = \text{Even} \end{cases}$	$N_{Switch} = \begin{cases} nU + 9, nU = Odd \\ nU + 8, nU = Even \end{cases}$
Number of Gate Driver	$N_{Driver} = \begin{cases} 8, & nU = 1 \\ nU + 9, & nU = \text{Odd} \quad nU > 1 \\ nU + 8, & nU = \text{Even} \end{cases}$	$N_{Driver} = \begin{cases} nU + 9, nU = \text{Odd} \\ nU + 8, nU = \text{Even} \end{cases}$
Maximum Blocking Voltage	$V_{Block} = (N_{Level} - 3) * V_{dc}$	$V_{Block} = (2nU + 1) * V_{dc}$
Total Peak Inverse Voltage	$V_{PIV} = ((6nU + 2) * V_{dc}$	$V_{PIV} = ((14nU + 2) * V_{dc}$

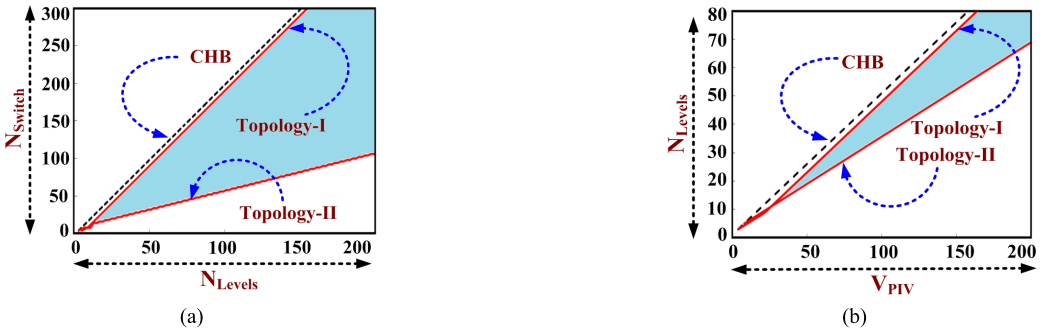


FIGURE 7. Comparison of symmetric configuration of Hybrid Topology I and II with Cascaded H-Bridge multilevel inverter (a) Graph of number of switches versus number of levels (b) Graph of number of levels versus Peak Inverse Voltage (PIV or V_{PIV}) of switch.

topology II is $n * V_{dc}$, and thus it is restricted to high power applications.

V. NEAREST LEVEL MODULATION SCHEME

Several high and low switching frequency modulation techniques proposed for multilevel converters such as multi-carrier PWM, Space Vector PWM, Selective Harmonic Elimination Method, hybrid modulation and fundamental switching. The nearest level control modulation technique used to control proposed inverter topologies is shown in Fig. 9. The switching sequence for topologies I and II are given in Table 5 and VI, respectively. L_1 to L_{12} are the comparator output, as shown in Fig. 9, and $\bar{L}_1$ to $\bar{L}_{12}$ is the NOT of the comparator output.

The switching logic equations for 27 level hybrid topology I are as follows,

$$P_1 = \left(L_1 \&\& \overline{L_2}\right) + \left(L_3 \&\& \overline{L_4}\right) + \left(L_6 \&\& \overline{L_7}\right) + \left(L_8 \&\& \overline{L_9}\right) + \left(L_{10} \&\& \overline{L_{11}}\right) + L_{12} \quad (9)$$

$$P_2 = \left(L_1 \&\& \overline{L_3}\right) + \left(L_7 \&\& \overline{L_9}\right) + \left(L_{10} \&\& \overline{L_{12}}\right) \quad (10)$$

$$H_1 = L_1 \&\& \overline{L_{11}} \quad (11)$$

$$H_1' = \left(L_1 \&\& \overline{L_5}\right) + L_9 \quad (12)$$

$$H_2' = \left(L_8 \&\& \overline{L_9}\right) \quad (13)$$

$$H_3' = \left(L_4 \&\& \overline{L_9}\right) \quad (14)$$

$$H_4' = L_9 \quad (15)$$

$$H_4 = \left(L_1 \&\& \overline{L_9}\right) + L_{10} \quad (16)$$

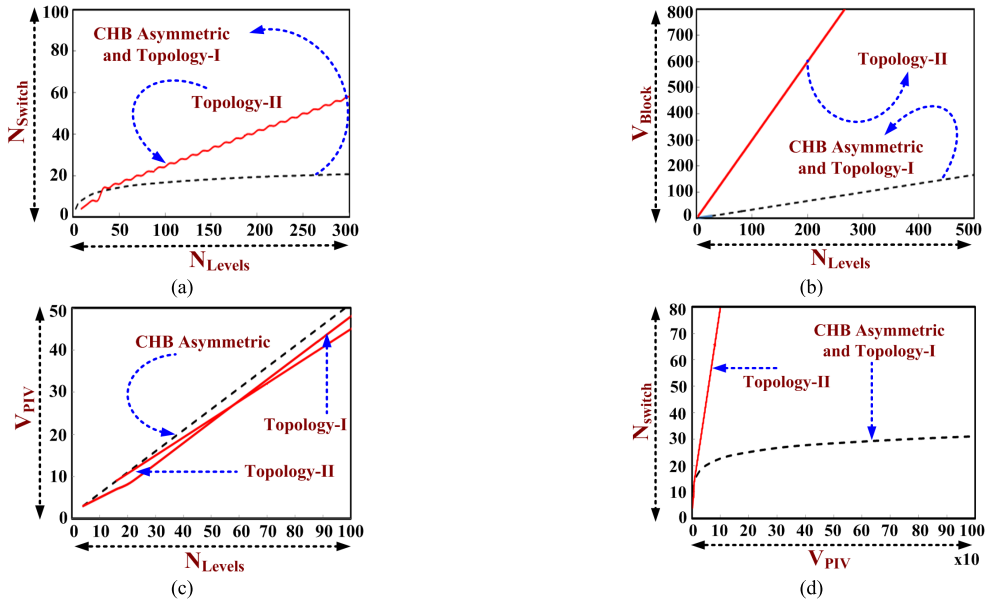


FIGURE 8. Comparison of asymmetric configuration of Hybrid Topology I and II with Cascaded H-Bridge multilevel inverter (a) Graph of number of switches versus number levels (b) graph of number of blocks versus number levels (c) graph of PIV or V_{PIV} of switch versus number levels (d) graph of number of switch versus PIV or V_{PIV} of switch.

TABLE 4. Comparison of symmetric configuration of multilevel inverter for maximum output voltage level against equal power component.

Description	CHB	[19]	[17]	Hybrid Topology I	Hybrid Topology II
Number of Level	13	17	23	17	35
Number of Switches (BUP400D)	24	24	24	24	24
Number of gate driver circuits (HCPL316j)	24	24	14	24	24
Number of ON state switches	12	12	4	12	11
THD %	6.39%	4.84%	3.56%	4.84%	2.33%

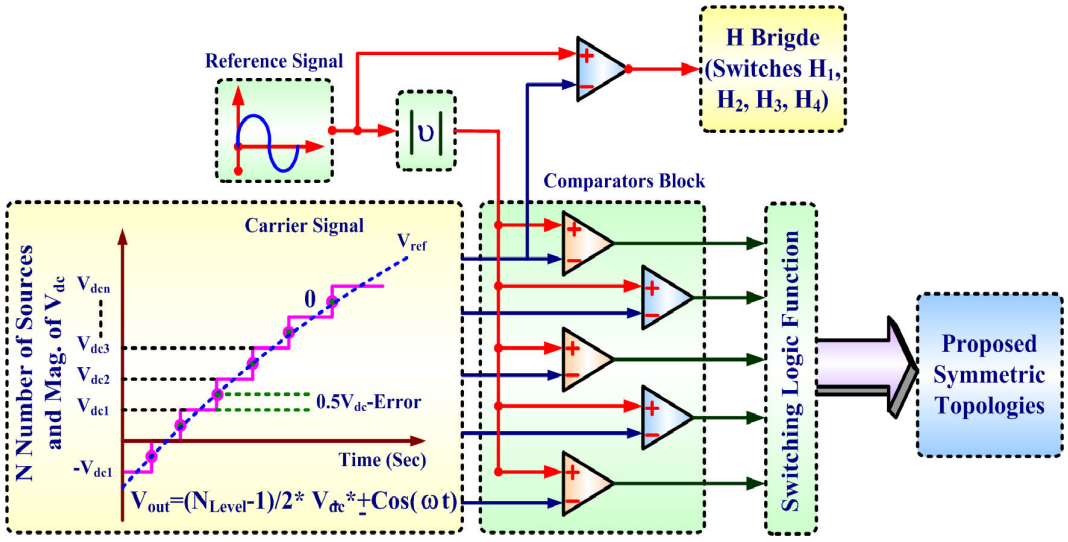


FIGURE 9. Schematic of nearest level control modulation technique to control proposed inverter.

The switching logic equations for 21 level hybrid topology II are as follows,

$$P_1 = (L_1 \&\& \overline{L_2}) + (L_3 \&\& \overline{L_4}) + (L_6 \&\& \overline{L_7}) + (L_8 \&\& \overline{L_9}) + (L_{10}) \quad (17)$$

$$P_2 = (L_1 \&\& \overline{L_3}) + (L_6 \&\& \overline{L_7}) + (L_8 \&\& \overline{L_9}) + (L_{10}) \quad (18)$$

$$H_1 = L_1 \quad (19)$$

$$H_4 = (L_1 \&\& \overline{L_7}) + L_8 \quad (20)$$

$$H_1' = (L_1 \&\& \overline{L_3}) + L_7 \quad (21)$$

TABLE 5. Switching sequence for proposed 27 level hybrid topology I.

Level	ON State Switches			Output Voltage
	Upper Leg	Upper Leg H Bridge	Lower Leg H Bridge	
0	-	H_1,H_2 or H_3, H_4	H_1', H_2' or H_3', H_4'	0 V
+1	P_1, P_2	H_1, H_4	H_1', H_2'	$+V_{14}$
+2	S_1, P_2	H_1, H_4	H_1', H_2'	$+V_{11}+V_{14}$
+3	S_2, P_1	H_1, H_4	H_1', H_2'	$+V_{12}+V_{13}+V_{14}$
+4	S_1, S_2	H_1, H_4	H_1', H_2'	$+V_{11}+V_{12}+V_{13}+V_{14}$
+5	S_1, S_2	H_1, H_4	H_2', H_3'	$-(+V_{11}+V_{12}+V_{13}+V_{14})+V_{21}$
+6	S_2, P_1	H_1, H_4	H_2', H_3'	$-(+V_{12}+V_{13}+V_{14})+V_{21}$
+7	S_1, P_2	H_1, H_4	H_2', H_3'	$-(+V_{11}+V_{14})+V_{21}$
+8	P_2, P_1	H_1, H_4	H_2', H_3'	$-(+V_{14})+V_{21}$
+9	-	H_1, H_2	H_1', H_4'	$+V_{21}$
+10	P_2, P_1	H_1, H_4	H_1', H_4'	$+V_{14}+V_{21}$
+11	S_1, P_2	H_1, H_4	H_1', H_4'	$+V_{11}+V_{14}+V_{21}$
+12	S_2, P_1	H_1, H_4	H_1', H_4'	$+V_{12}+V_{13}+V_{14}+V_{21}$
+13	S_1, S_2	H_1, H_4	H_1', H_4'	$+V_{11}+V_{12}+V_{13}+V_{14}+V_{21}$
-13	S_1, S_2	H_2, H_3	H_2', H_3'	$-(+V_{11}+V_{12}+V_{13}+V_{14})-V_{21}$
-12	S_2, P_1	H_2, H_3	H_2', H_3'	$-(+V_{12}+V_{13}+V_{14})-V_{21}$
-11	S_1, P_2	H_2, H_3	H_2', H_3'	$-(+V_{11}+V_{14})-V_{21}$
-10	P_2, P_1	H_2, H_3	H_2', H_3'	$-V_{14}-V_{21}$
-9	-	H_2, H_3	H_2', H_3'	$-V_{21}$
-8	P_2,P_1	H_2, H_3	H_1', H_4'	$(+V_{14})-V_{21}$
-7	S_1,P_2	H_2, H_3	H_1', H_4'	$(+V_{11}+V_{14})-V_{21}$
-6	S_2,P_1	H_2, H_3	H_1', H_4'	$(+V_{12}+V_{13}+V_{14})-V_{21}$
-5	S_1,S_2	H_2, H_3	H_1', H_4'	$(+V_{11}+V_{12}+V_{13}+V_{14})-V_{21}$
-4	S_1,S_2	H_2,H_3	H_3', H_4'	$-(+V_{11}+V_{12}+V_{13}+V_{14})$
-3	S_2,P_1	H_2, H_3	H_3', H_4'	$-(+V_{12}+V_{13}+V_{14})$
-2	P_2, S_1	H_2, H_3	H_3', H_4'	$-(+V_{11}+V_{14})$
-1	P_2,P_1	H_2, H_3	H_3', H_4'	$-(V_{14})$

TABLE 6. Switching sequence for proposed 21 level hybrid topology II.

Level	ON State Switches			Output Voltage
	Upper Leg	Upper Leg H Bridge	Lower Leg H Bridge	
0	-	H_1,H_2 or H_3, H_4	H_1', H_2' or H_3', H_4'	0 V
+1	P_2,P_1	H_1,H_4	H_1', H_2'	$+V_{13}$
+2	P_2, S_1	H_1,H_4	H_1', H_2'	$+V_{11}+V_{13}$
+3	S_2,P_1	H_1,H_4	H_1', H_2'	$+V_{12}+V_{13}+V_{11}$
+4	S_2,P_1	H_1,H_4	H_2', H_3'	$-(+V_{12}+V_{13}+V_{11})+V_{21}$
+5	S_1,P_2	H_1,H_4	H_2', H_3'	$-(+V_{11}+V_{12})+V_{21}$
+6	P_2,P_1	H_1,H_4	H_2', H_3'	$-(+V_{11})+V_{21}$
+7	-	H_1,H_2	H_1', H_4'	$+V_{21}$
+8	P_2,P_1	H_1,H_4	H_1', H_4'	$+V_{13}+V_{21}$
+9	S_1,P_2	H_1,H_4	H_1', H_4'	$+V_{11}+V_{12}+V_{21}$
+10	S_2,P_1	H_1,H_4	H_1', H_4'	$+V_{12}+V_{13}+V_{11}+V_{21}$
-10	S_2,P_1	H_2,H_3	H_2', H_3'	$-(+V_{12}+V_{13}+V_{11})-V_{21}$
-9	S_1,P_2	H_2,H_3	H_2', H_3'	$-(+V_{11}+V_{12})-V_{21}$
-8	P_2,P_1	H_2,H_3	H_2', H_3'	$-V_{13}-V_{21}$
-7	-	H_2,H_3	H_2', H_3'	$-V_{21}$
-6	P_2,P_1	H_2,H_3	H_1', H_4'	$(+V_{13})-V_{21}$
-5	S_1,P_2	H_2,H_3	H_1', H_4'	$(+V_{11}+V_{13})-V_{21}$
-4	S_2,P_1	H_2,H_3	H_1', H_4'	$(+V_{12}+V_{13}+V_{11})-V_{21}$
-3	S_2,P_1	H_2,H_3	H_3', H_4'	$-(+V_{12}+V_{13}+V_{11})$
-2	P_2, S_1	H_2,H_3	H_3', H_4'	$-(+V_{13}+V_{12})$
-1	P_2,P_1	H_2,H_3	H_3', H_4'	$-(V_{13})$

$$H_2' = L_6 \tag{22}$$

$$H_3' = \left(L_4 \&\& \overline{L_7}\right) \tag{23}$$

$$H_4' = L_7 \tag{24}$$

For the negative half cycle, the same logic function with the corresponding comparator signal given. This modulation technique operates under the fundamental switching frequency method. The fundamental switching method has low switching losses compared to other modulation strategies.

The THD is another important measuring factor in the multilevel converter, which calculates the percentage of harmonic content present in the output waveform.

In general, the THD for the sinusoidal waveform calculated as follows:

$$THD = \frac{\sqrt{\left(\sum_{h=3,5,7.....}^{\infty} V_{oh}\right)}}{V_{of}} = \sqrt{\left(\frac{V_{orms}}{V_{of}}\right)^2 - 1} \tag{25}$$

TABLE 7. Comparison of the asymmetric configuration for equal number of level against number of power switches.

Description	CHB Asymmetric	Hybrid Topology I Asymmetric	Hybrid Topology II Asymmetric	[16]
Number of Level	81	81	81	81
Number of Switches (BUP400D)	16	16	22	32
Number of gate driver Circuits (HCPL316j)	16	16	22	20
Maximum Blocking Voltage	$27V_{dc}$	$27V_{dc}$	$27V_{dc}$	$27\ V_{dc}$
Total Peak Inverse Voltage	$160V_{dc}$	$166V_{dc}$	$184V_{dc}$	$274V_{dc}$
Variety of DC Source	4	3	2	2

where V_{orms} and V_{of} denote the magnitude of rms value and fundamental output voltage waveform, respectively. The V_{rms} and V_{of} calculated with the help of switching angles. The formula for finding switching angle represented as follows,

$$\theta_i = \sin^{-1}\left(\frac{i-0.5}{N_{Level}}\right) \quad i = 1, 2, 3 \ldots N_{Level} \tag{26}$$

The THD of the output voltage waveform depends on the number of levels and switching angles, which is not the case of current waveform because the inductive load acts as a low pass filter and brings to sinusoidal shape. The V_{out} of the proposed topology represented as,

$$V_{out} = (N_{Level} - 1)\ /2^* V_{dc}{}^* \pm (cos\ \omega t) \tag{27}$$

VI. EXPERIMENTAL RESULTS

For analyze the operation of proposed topologies, the experimental test has conducted and results discussed. The nearest level control technique used to generate the appropriate gate pulses for the switches. For verify the performance of the proposed multilevel converter, an experimental prototype based on the primary unit configuration is developed for a resistive-inductive load of $R = 65\ \Omega$ and $L = 40$ mH. Moreover, the conventional nearest-voltage level modulation technique, presented in [17], is embedded in the FPGA Spartan XE3S250E controller (that generates the trigger pulses to the appropriate switches) with a fundamental frequency of 50 Hz.

A. HYBRID TOPOLOGY I (ASYMMETRIC CONFIGURATION)

The 27-level hybrid topology I multilevel converter is simulated using MATLAB/Simulink and SimPower Systems toolbox for the proposed topologies. Topology I, asymmetric

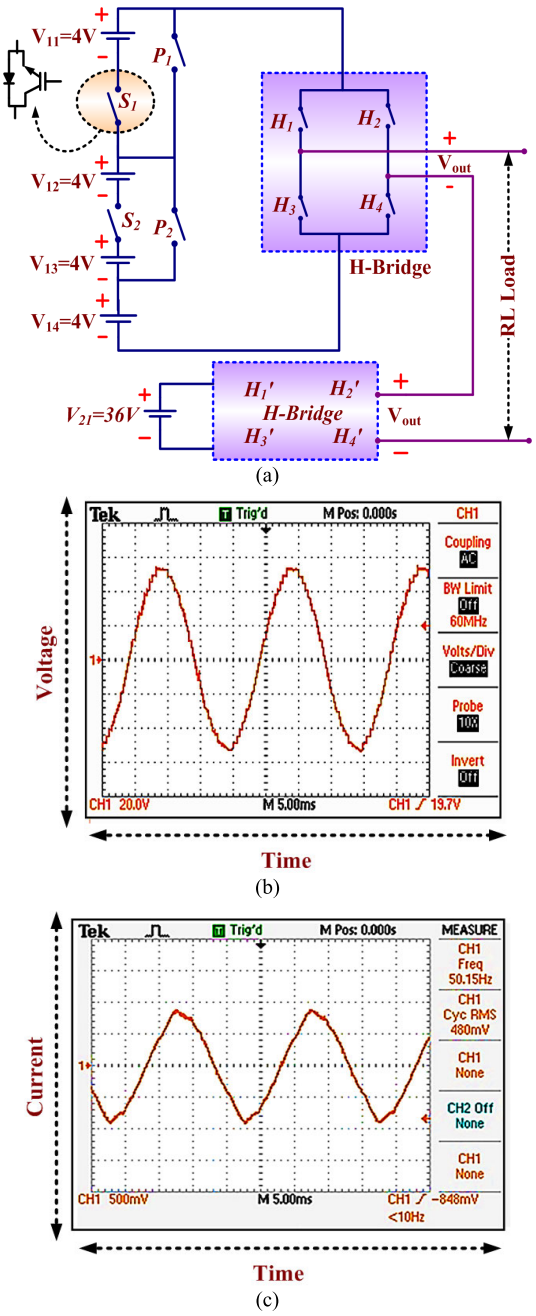
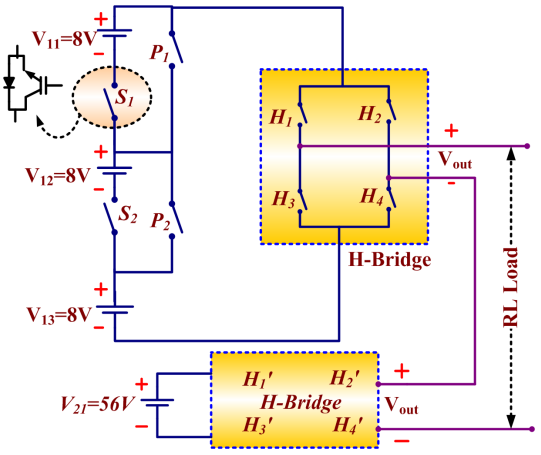
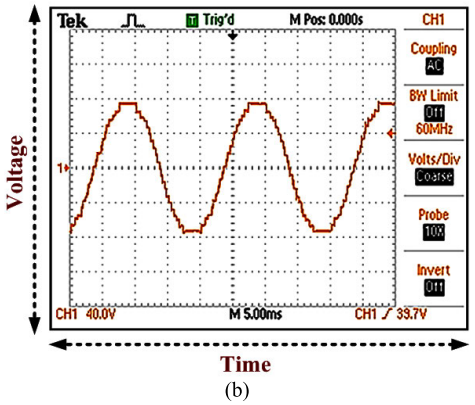


FIGURE 10. Experimental circuit and result of Hybrid Topology I (a) Power circuit of 27 level Hybrid Topology I (b) Output voltage waveform (c) Output current waveform.

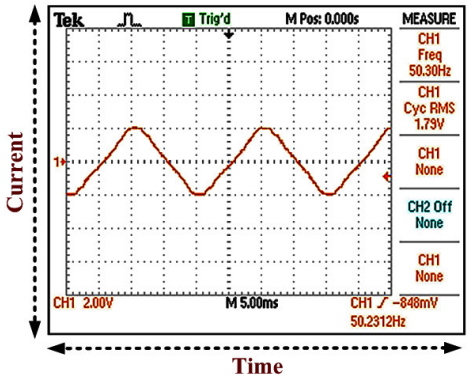
configuration showed in Fig. 10(a), the magnitude of dc sources of basic unit is $V_{11} = V_{12} = V_{13} = V_{14} = 4$ V and the full-bridge converter voltage $V_{21} = 36$ V for the resistive-inductive load value of 50 Ω and 60 mH. The hardware experimental output voltage and current waveform showed in Fig. 10(b) and Fig. 10(c), respectively. In hybrid topology, I, the maximum blocking voltage of the lower is 36 V, and upper leg is 16 V, the total peak inverse voltage is 232 V whereas in CHB trinary configuration uses 208 V,



(a)



(b)



(c)

FIGURE 11. Experimental Result of Hybrid Topology II (a) Power Circuit of 21 level Hybrid Topology II (b) Output voltage waveform (c) Output current waveform.

in case of topology [16]–[19] uses a higher number of blocking voltages.

B. HYBRID TOPOLOGY II (ASYMMETRIC CONFIGURATION)

The hybrid topology II asymmetric configuration is shown in Fig. 11(a). The magnitude of dc sources of basic unit is $V_{11} = V_{12} = V_{13} = 8$ V and the full-bridge converter voltage $V_{21} = 56$ V for the resistive-inductive load value of 30 Ω and 45 mH. This topology is more suitable for the reduction

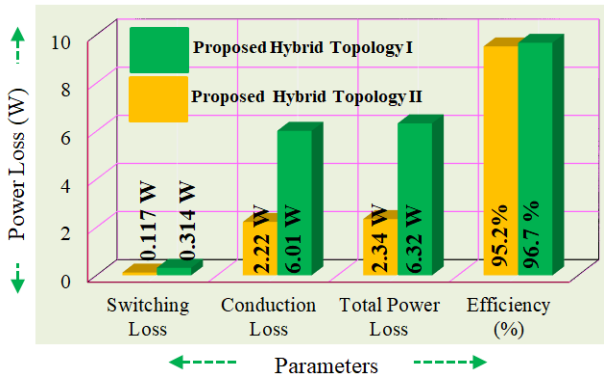


FIGURE 12. Plot of power Loss and efficiency.

of a variety of dc source because it uses two varieties of dc source for m-levels and the total peak inverse voltage is close to topology I and CHB. The hardware experimental output voltage and current waveforms are shown in Fig. 11(b) and Fig. 11(c). The maximum blocking voltage of upper leg full bridge converter is 24 V and lower leg is 56 V and total peak inverse voltage is 352 V.

Table 5 describes the equal number of levels produces by the various topologies with the different switch count. It is once again proved that the proposed topology I and CHB produces the same number of voltage level, whereas topology II and [16]–[19] uses a large number of switches. The maximum blocking voltage of all the topologies is the same; but, the total peak inverse voltage is higher in [16]–[19] due to various rating of bidirectional switches used. The plots of power loss and efficiency of the proposed topology given in Fig. 12, which shows that the proposed hybrid topology I have higher efficiency compared with topology II.

VII. CONCLUSION

In this article, a new single/double source unit-based hybrid multilevel converter topologies proposed for medium applications. The proposed multilevel converter uses a minimum number of power switches. The comparison of hybrids proposed symmetric and asymmetric topologies presented in terms of the number of switches, the number of gate driver circuits and total peak inverse voltage. These factors reduce the size of the circuit, installation area and total cost of the converter. In the symmetric configuration, the proposed hybrid topologies are superior to the conventional topology, but in case of asymmetric configuration, the proposed hybrid topology I and CHB use an equal number of switches for same output voltage level.

The proposed basic multilevel inverter and hybrid topology II are not suitable for high voltage applications due to restriction of maximum voltage stress on the full-bridge converter, and these topologies are suitable for medium voltage application like 2.0 kV -to- 6.0 kV grid-connected photovoltaic system. The proposed hybrid Topology I is suggested for high voltage applications because it is closer

to conventional CHB with increased stepped output voltage level as compared to conventional CHB topology.

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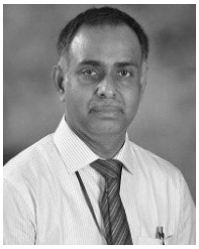

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